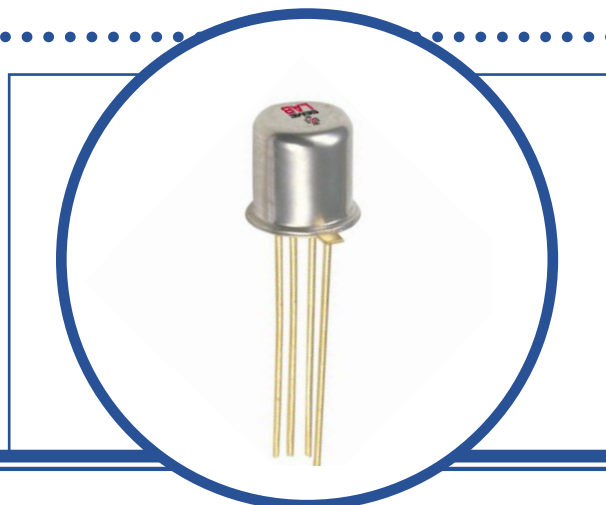


SILICON SMALL SIGNAL N-CHANNEL JFET

2N3823

- Low Noise, High Gain.
- TO-72 Hermetic Package
- Excellent High Frequency Gains
- Screening Options Available.



ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise stated)

V_{DS}	Drain – Source Voltage	30V
V_{DG}	Gate – Drain Voltage	30V
V_{GS}	Gate – Source Voltage	-30V
I_G	Gate Current	10mA
P_D	Total Power Dissipation at $T_A = 25^\circ\text{C}$ Derate Above 25°C	300mW 1.7mW/ $^\circ\text{C}$
T_J	Junction Temperature Range	-55 to $+200^\circ\text{C}$
T_{stg}	Storage Temperature Range	-55 to $+200^\circ\text{C}$

Semelab Limited reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.



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SILICON SMALL SIGNAL N-CHANNEL JFET 2N3823

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise stated)

Symbols	Parameters	Test Conditions	Min.	Typ	Max.	Units
$V_{(BR)GSSR}$	Gate – Source Breakdown Voltage	$V_{DS} = 0$ $I_G = 1.0\mu\text{A}$	30			V
I_{DSS}^1	Saturation Drain Current	$V_{DS} = 15\text{V}$ $V_{GS} = 0$	4		20	mA
V_{GS}	Gate – Source Voltage	$V_{DS} = 15\text{V}$ $I_D = 400\mu\text{A}$	1		7.5	V
$V_{GS(off)}$	Gate – Source Cut-off Voltage	$V_{DS} = 15\text{V}$ $I_D = 50\mu\text{A}$			8	V
I_{GSSR}	Gate Reverse Current	$V_{DS} = 0$ $V_{GS} = -20\text{V}$			0.5	nA
		$T_A = +150^\circ\text{C}$			0.5	μA

DYNAMIC CHARACTERISTICS

$ g_{fs} ^1$	Common – Source Forward Transconductance	$V_{DS} = 15\text{V}$ $V_{GS} = 0$	3.5		6.5	mS
		$f = 1.0\text{KHz}$ $T_A = -55^\circ\text{C}$			9.75	
		$V_{DS} = 15\text{V}$ $V_{GS} = 0$	3.2 ²			
		$f = 200\text{MHz}$				
g_{os}^1	Common – Source Output Transconductance	$V_{DS} = 15\text{V}$ $V_{GS} = 0$			35	μS
		$f = 1.0\text{KHz}$				
NF1	Common-source spot noise figure	$V_{DS} = 15\text{V}$ $V_{GS} = 0$			2.5 ²	dB
		$R_G = 1\text{K}\Omega$ $f = 105\text{MHz}$				
C_{iss}	Common – Source Input Capacitance	$V_{DS} = 15\text{V}$ $V_{GS} = 0$			6	pF
C_{rss}	Common – Source Reverse Transfer Capacitance	$f = 1.0\text{MHz}$			2	

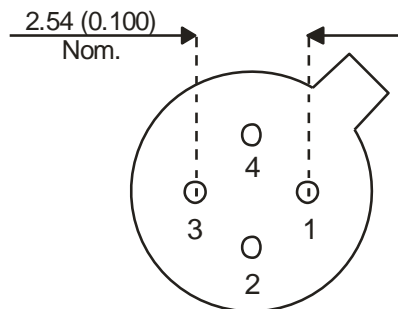
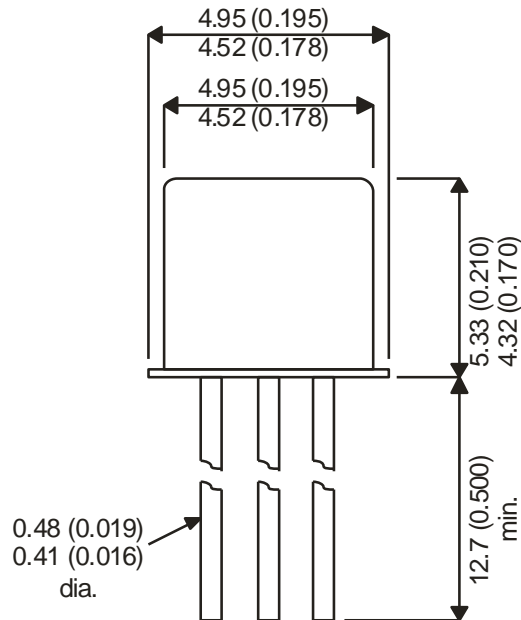
¹ Pulse Width $\leq 300\mu\text{s}$, $\delta \leq 2\%$

² By design only, not a production test

SILICON SMALL SIGNAL N-CHANNEL JFET 2N3823

MECHANICAL DATA

Dimensions in mm (inches)



TO-72 (TO-206AF)

PIN1 – SOURCE

PIN2 – DRAIN

PIN3 – GATE

PIN4 - CASE